

SPVC1010RH

10 A, 40 V ADJUSTABLE VOLTAGE CLAMP



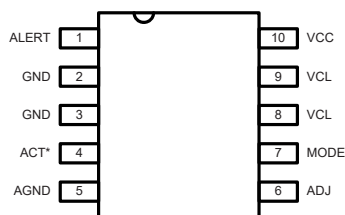
FEATURES

- Up to 10 A shunt regulator automatically activated
- > 18 W power dissipation capability (10 ms)
- VCC operating voltage: 3 V ... 40 V
- Adjustable clamp voltage:
 - 3 V ... 40 V : VCC connected to protected voltage
 - 0.8 V ... 40 V : VCC separately supplied
- Internal 0.8 V ($\pm 1.5\%$) reference
- Active shunt flag inverted output (ACT*)
- Over-current, over-temperature and over-voltage detection
- Standby current < 200 μ A
- LDR TID > 100 krad (Si)
- SEE tolerant LET ≤ 60 MeV \cdot cm²/mg
- Latch-up immune (fully isolated SOI technology)
- Hermetic dual in-line 10-lead flatpack package
- Screened according to ESCC
- Extended temperature range: -55 °C to +125 °C

APPLICATIONS

- Power conversion and distribution systems
- Satellite systems and launch vehicles

PIN DIAGRAM



DESCRIPTION

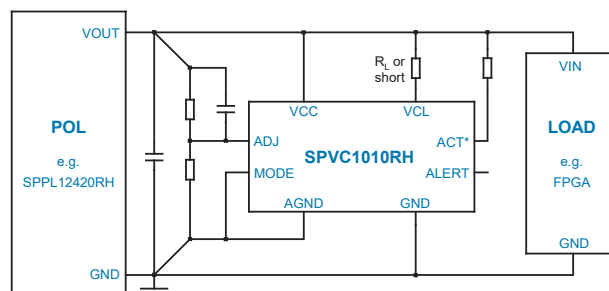
The SPVC1010RH is a radiation hardened adjustable voltage clamp designed to protect a power supply load in the event of an overvoltage. The SPVC1010RH contains a shunt regulator which, under an overvoltage condition, regulates the output voltage to the adjusted maximum value.

The SPVC1010RH compares a divided down portion of the power supply output to an internal reference. If the divided output voltage is below the internal reference the SPVC1010RH remains in standby mode. If it is above the SPVC1010RH shunts up to 10 A to keep the voltage within the adjusted limit and activates the ACT* signal.

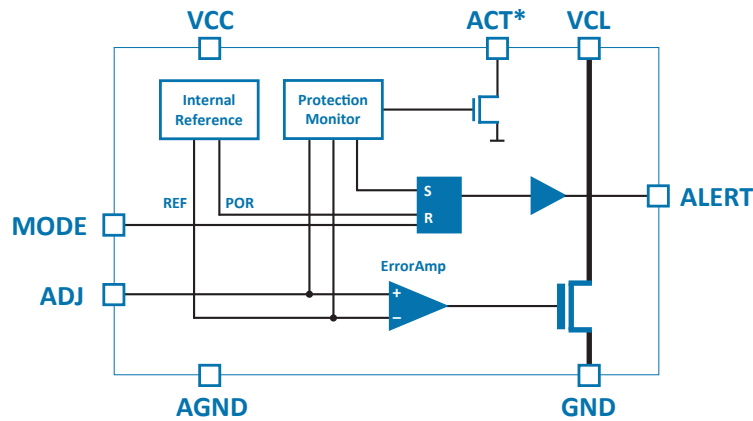
If the shunted current exceeds the overcurrent threshold or the chip junction temperature exceeds 165 °C or V_{ADJ} exceeds the overvoltage threshold, the ALERT output becomes activated which can be used in flag-mode or latch-mode as flag signal or to switch an external power transistor.

The device is packaged in a hermetically sealed 10-pin flatpack with straight leads.

TYPICAL APPLICATION



FUNCTIONAL BLOCK DIAGRAM



ALERT LOGIC TABLE

DETECTION MODE	MODE INPUT	ALERT OUTPUT	over-current OR over-temperature OR over-voltage		LATCHED
			L	H	
latch-mode	H	push-pull	0V	VCC	yes
flag-mode	L	open-drain	high-Z	0V	no

PIN DESCRIPTIONS

PIN NAME	PIN NUMBER	PIN DESCRIPTION
ALERT	1	Alert output pin: The ALERT pin is a switchable push-pull driver / open-drain output pin configured by the MODE input. In latch-mode it assigns high (VCC voltage) in case of latched over-current, over-temperature or over-voltage condition. It can be used as a flag and to drive an external power switch transistor for immediate shutdown. The latched ALERT condition becomes released by power-on reset or by the MODE input. In flag-mode ALERT operates as open-drain output and assigns low in case of (unlatched) over-current, over-temperature or over-voltage condition.
GND	2 - 3	Ground pin. The package lid is connected to GND.
ACT*	4	Active shunt flag pin: Open-drain output which asserts low if the ADJ voltage exceeds the threshold of 0.8 V and the shunt regulator draws current at the VCL pins.
AGND	5	Analog ground pin. To be used according to typical application circuit only.
ADJ	6	Clamp voltage adjustment input pin: The ADJ pin senses the divided output voltage to regulate and clamp that voltage. Drive the ADJ pin with a resistive voltage divider from the output voltage. The adjustment threshold is 0.8 V.
MODE	7	Detection mode input pin with internal pull-down: When MODE is high the over-current, over-temperature and over-voltage detection operates in latch-mode and the ALERT output is configured as push-pull driver. When MODE is low the latched over-current / over-temperature / over-voltage alert becomes released respectively the detection operates in flag-mode and the ALERT output is configured as open-drain driver.
VCL	8 - 9	Power input pin: The VCL pin is the power input of the SPVC1010RH. It can be operated up to 40 V and draws up to 10 A when the shunt regulator is active. The instantaneous current is a function of the control loop sensing the changes at ADJ.
VCC	10	Supply pin: The VCC pin supplies the input voltage to the internal reference, regulator and protection circuits. The voltage clamping works properly if the VCC pin voltage is in the range from 3 V to 40 V. Below 3V the chip is in standby.

ABSOLUTE MAXIMUM RATINGS (NOTE1)

Input voltage range (all pins) -0.3 V to +40 V
 Lead temperature (soldering, 10s) +300 °C
 Storage temperature range -65 °C to +150 °C
 ESD Rating (HBM) 4 kV

NOTE1 Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

V_{VIN} - Supply voltage +3 V to +40 V
 V_{VCL} - Clamp voltage +0.8 V to +40 V
 T_A - Operating ambient temperature range -55 °C to +125 °C
 T_J - Operating junction temperature..... $\leq +150$ °C

RADIATION HARDNESS

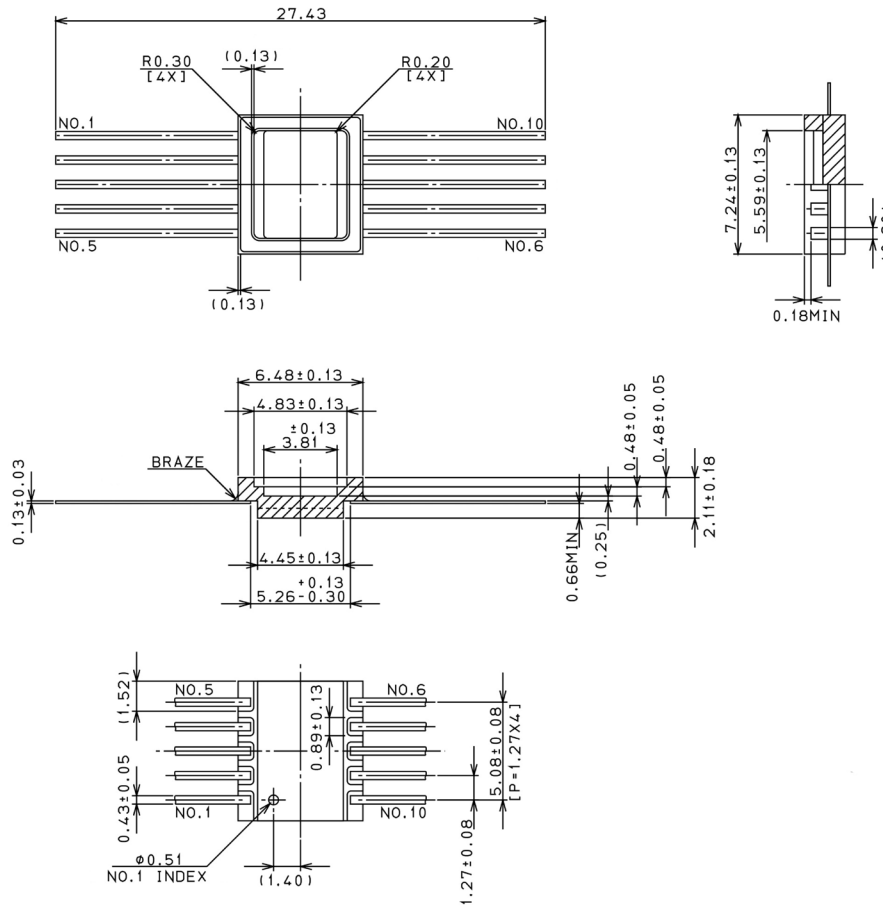
LDR TID 100 krad (Si)
 Free from SET and destructive SEE 60 MeV·cm²/mg
 SEL, SEFI and SEU immune

ELECTRICAL CHARACTERISTICS

Typical values at $T_A = 25$ °C. All voltages with respect to GND / AGND.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{VCL}	Clamp voltage		0.8		40	V
V_{VCC}	Supply voltage		3		40	V
$I_{VCC,Z}$	Supply current, standby	$V_{VCC} = 10$ V, ACT* = H	140	160	200	μA
I_{VCC}	Supply current, active	$V_{VCC} = 10$ V, ACT* = L	500	700	800	μA
V_{REF}	Reference voltage	$I_{VCL} = 20$ mA	0.789	0.8	0.811	V
dV_{LOAD}	Load regulation	0.02 A $< I_{VCL} < 10$ A, $V_{VCL} = 3$ V	-0.1		0.1	%/A
dV_{LINE}	Line regulation	3 V $< V_{VCC} = V_{VCL} < 10$ V, $I_{VCL} = 20$ mA	-0.05		0.05	%/V
I_{ADJ}	ADJ input leakage		-1		1	μA
I_{SINK}	ACT*, ALERT sink current		6	8	12	mA
I_{SOURCE}	ALERT source current		-16	-10	-5	mA
$R_{VCL,ON}$	VCL $R_{DS,ON}$ resistance	$V_{ADJ} > V_{REF}$, $I_{VCL} = 1$ A			100	mΩ
$I_{VCL,Oth}$	VCL over-current threshold		10			A
T_{LIM}	Over-temperature threshold			165		°C
$V_{ADJ,OVth}$	Over-voltage threshold	$V_{ADJ} > V_{REF}$	0.870	0.895	0.920	V
$V_{CC,UVth}$	VCC under-voltage threshold voltage	V_{CC} falling		2.7		V
$V_{CC,UVhys}$	VCC under-voltage threshold voltage hysteresis			100		mV
$V_{MODE,th}$	MODE threshold	V_{MODE} rising	0.9	1.0	1.1	V
$V_{MODE,th}$	MODE threshold hysteresis			100		mV

PACKAGE DIMENSION (10-LEAD FLATPACK)



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