SPLVDS032RH

Quad LVDS Line Receiver with Extended Common Mode

FEATURES

- DC to 400 Mbps / 200 MHz low noise, low skew, low power operation
  - 400 ps (max) channel-to-channel skew
  - 300 ps (max) pulse skew
  - 7 mA (max) power supply current
- LVDS inputs conform to TIA/EIA-644-A standard
- Extended input common mode voltage range: -7 V to +12 V
- Radiation hardness
  - TID > 50 krad (Si)
  - SEE (except SET): LET > 60 MeV / (mg / cm^2)
  - SET: LET > 12.7 MeV / (mg / cm^2)
- Latch-up immune due to dielectric isolation
- Hermetic dual in-line 16-lead flatpack package
- Screened according to ESCC
- Open or undriven fail-safe support
- Pin compatible with UT54LVDS032LV
- Extended temperature range -55 °C to +125 °C

DESCRIPTION

The SPLVDS032RH is a radiation hardened 400 Mbps Quad LVDS (low voltage differential signaling) Line Receiver optimized for high-speed, low power, low noise transmission over controlled impedance (approximately 100 Ω) transmission media (e.g. cables, printed circuit board traces, backplanes). The SPLVDS032RH accepts four LVDS signals and translates them to four LVCMOS signals. The outputs can be disabled and put in a high-impedance state via two enable pins, OE and OE*.

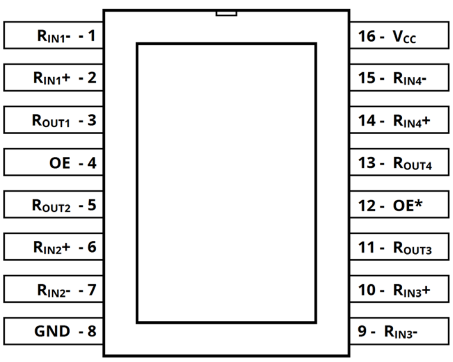
The SPLVDS032RH input receivers support wide input voltage range of -7.5 V to +12.5 V for exceptional noise immunity comparable to RS-485. A fail-safe feature sets the outputs to a high state when both inputs are open or undriven.

Supply current is 7 mA (max). LVDS inputs conform to the ANSI/EIA/TIA-644-A standard. The SPLVDS032RH is offered in 16-lead flatpack package and operates over an extended -55 °C to +125 °C temperature range.

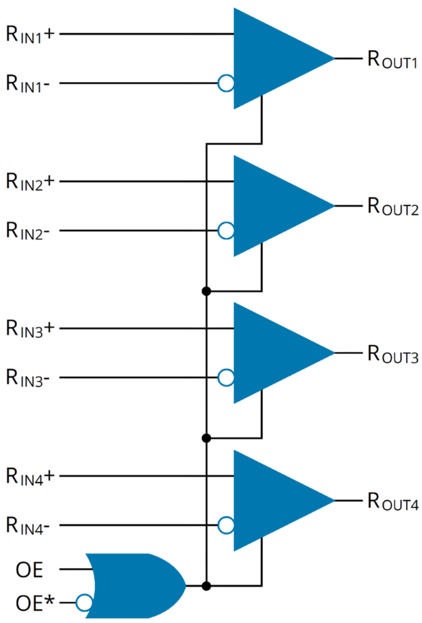
APPLICATIONS

- Data Communications
- SpaceWire Links
- Satellite Systems
- Launch Vehicles

PIN DIAGRAM



FUNCTION DIAGRAM



LOGIC TABLE

OE	OE*	$R_{IN}+ - R_{IN}-$	R_{OUT}
Any other combination		≥ 100 mV	H
		≤ -100 mV	L
		Failsafe condition	H
0	1	Don't Care	Disabled

PIN DESCRIPTIONS

PIN NAME	PIN NUMBER	PIN TYPE	PIN DESCRIPTION
$R_{IN1}+$, $R_{IN1}-$, $R_{IN2}+$, $R_{IN2}-$, $R_{IN3}+$, $R_{IN3}-$, $R_{IN4}+$, $R_{IN4}-$	2, 1, 6, 7, 10, 9, 14, 15	LVDS inputs	Non-inverting and inverting LVDS receiver input pins.
R_{OUT1}, R_{OUT2}, R_{OUT3}, R_{OUT4}	3, 5, 11, 13	LVCMOS outputs	Receiver LVCMOS output pins.
OE, OE*	4, 12	LVCMOS inputs	Receiver output enable pins. When OE is high or OE* is low or open, the receiver outputs are enabled. When OE is low and OE* is high, the receiver outputs are disabled.
VCC	16	Power	Power supply pin. Bypass Vcc to GND with 0.1 µF and 0.01 µF ceramic capacitors.
GND	8	Power	Ground or circuit common pin.

ABSOLUTE MAXIMUM RATINGS *(NOTE1)*

V_{CC} to GND.................................... -0.3 V to +4 V
Inputs
OE, OE* to GND................... -0.3 V to V_{CC} + 0.3 V
R_{IN}+, R_{IN}- to GND .... -8.0 V to +13.0 V
V_{ID} (R_{IN}+ to R_{IN}-) .... -6.0 V to +6.0 V
Outputs
R_{OUT} to GND........................ -0.3 V to V_{CC} + 0.3 V

16-Lead Flatpack Thermal Resistance ***(NOTE2)***
θ_{JC} .... 10 °C/W

T_J - Maximum Junction Temperature........... +150 °C
T_L - Lead Temperature (soldering, 4 s) .... +260 °C
T_{stg} - Storage Temperature Range.....-65 °C to +150 °C

ESD Ratings
HBM[1] .... 8 kV

[1] Human Body Model, applicable standard JESD22-A114-C

NOTE1 *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
NOTE2 *Thermal resistance junction to case.*

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Pins	MIN	TYP	MAX	Unit
V_{CC}	Supply voltage	V_{CC}	3.0	3.3	3.6	V
V_{IH}	High-level input voltage	OE, OE*	2.0		V_{CC}	V
V_{IL}	Low-level input voltage	OE, OE*	0		0.8	V
V_{ID}	Differential input voltage	R_{IN}+, R_{IN}-	0.1	0.35	1	V
V_{IN}	Input voltage	R_{IN}+, R_{IN}-	-7.5		12.5	V
T_C	Case temperature range		-55	25	125	°C

ELECTRICAL CHARACTERISTICS

Recommended operating conditions, T_C = 25 °C, V_{CC} = 3.3V, unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
LVCMOS Input Specifications (OE, OE* pins)						
V_{IH}	High-level input voltage		2.0		V_{CC}	V
V_{IL}	Low-level input voltage		GND		0.8	V
I_{IH}	High-level input current	V_{CC} = 3.6 V V_{IN} = 3.6 V	-10		10	μA
I_{IL}	Low-level input current	V_{CC} = 3.6 V V_{IN} = 0 V	-10		10	μA
V_{CL}	Input clamp voltage ***(NOTE4)***	I_{CL} = -18 mA, V_{CC} = 0 V	-1.5	-0.9		V

ELECTRICAL CHARACTERISTICS (CONTINUED)

Over recommended operating conditions, T_C = 25 °C, V_{CC} = 3.3V, unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
LVCMOS Output Specifications (R_{OUT} pins)						
V_{OH}	Output high voltage	I_{OH} = -0.4 mA, V_{ID} = 200 mV	2.7	3.2		V
		I_{OH} = -0.4 mA, input open	2.7	3.2		V
V_{OL}	Output low voltage	I_{OL} = 2 mA, V_{ID} = -200 mV		0.05	0.25	V
I_{OS}	Output short circuit current *(NOTE3), (NOTE5)*	Enabled, V_{OUT} = 0 V or V_{CC}	-100		100	mA
I_{OZ}	Output High-Z current	Disabled, V_{OUT} = 0 V or V_{CC}	-10		10	µA
LVDS Input Specifications (R_{IN}+, R_{IN}- pins)						
V_{TH}	Differential input high threshold	V_{ICM} = -7.0 V to 12.0 V *(NOTE6)*		0	100	mV
V_{TL}	Differential input low threshold		-100	0		mV
V_{ID}	Differential input voltage		0.1	0.35	1	V
V_{ICM}	Input common mode voltage	V_{ID} = 100 mV	-7.0		12.0	V
I_{IN}	Input current, V_{CC} = 0 or 3.6 V	0 V ≤ V_{IN}+ ≤ 2.4 V, V_{IN}- = 1.2 V	-15		20	µA
		-4 V ≤ V_{IN}+ ≤ 6.4 V, V_{IN}- = open	-50		50	µA
		-7 V ≤ V_{IN}+ ≤ 12 V, V_{IN}- = open	-110		150	µA
C_{IN}	Input capacitance *(NOTE4)*	R_{IN}+ or R_{IN}- to GND		4		pF
Power Supply Current Specifications						
I_{CC}	Power supply current	Enabled, not switching		5	7	mA
I_{CCZ}	Power supply current with disabled outputs	Disabled		1	2	mA

NOTE3 *Current into device pin is defined as positive. Current out of the device is defined as negative.*

All voltages are referenced to ground, unless otherwise specified.

NOTE4 *This specification is not production tested and is guaranteed by design simuiations.*

NOTE5 *Output short circuit current (I_{OS}) is specified for output shorted to VCC or GND where the current direction is indicated by the polarity. Only one output should be shorted at a time, do not exceed maximum junction temperature specification. Specified for momentary short condition durations only.*

NOTE6 *Recommended operating conditions for the R_{IN}+ and R_{IN}- pins is over the range of -7.0 V to 12.0 V. Therefore, caution should be taken not to exceed these values or the maximum Differential input voltage of 1.0 V.*

SWITCHING CHARACTERISTICS

Over recommended operating conditions, T_C = 25 °C, V_{CC} = 3.3V, unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
LVDS AC Specifications ***(NOTES 7, 8)***						
t_{PLH}	Propagation delay, low-to-high	C_L = 15 pF, V_{ID} = 200 mV, V_{ICM} = 1.2 V ***(NOTE13)*** Figures 1 and 2	1.3	2.1	3.3	ns
t_{PHL}	Propagation delay, high-to-low		1.3	2.1	3.3	ns
t_r	Rise time			0.35	1	ns
t_f	Fall time			0.3	1	ns
$t_{SK(p)}$	Pulse skew ***(NOTE9)***			50	300	ps
$t_{SK(c-c)}$	Channel-to-channel skew ***(NOTE10)***			100	400	ps
$t_{SK(p-p)}$	Part-to-part skew ***(NOTE11)***				1.5	ns
t_{PLZ}	Disable time, low-to-high Z	R_L = 2 kΩ, C_L = 15 pF, V_{ID} = 200 mV, V_{ICM} = 1.2 V ***(NOTE13)*** Figures 3 and 4		8	14	ns
t_{PHZ}	Disable time, high-to-high Z			8	14	ns
t_{PZL}	Enable time, high Z-to-low			8	14	ns
t_{PZH}	Enable time, high Z-to-high			8	14	ns
f_{MAX}	Maximum operating frequency ***(NOTE12, NOTE13)***		200			MHz

NOTE7 *Generator output characteristics (unless otherwise specfied): f = 1 MHz, Z_0 = 50Ω, t_r < 1 ns, t_f < 1 ns.*

NOTE8 *Switching Characteristic specifications are not production tested and are guaranteed by statistical analysis of characterization data.*

NOTE9 *$t_{SK(p)}$, pulse skew, is the magnitude difference in propagation delay time between the positive going edge and the negative going edge of the same channel ($t_{SK(p)} = |t_{PLH} - t_{PHL}|$).*

NOTE10 *$t_{SK(c-c)}$, channel-to-channel skew, is the difference in propagation delay time between channels on the same device at any operating temperature and supply voltage.*

NOTE11 *$t_{SK(p-p)}$, part-to-part skew, is the difference in propagation delay time between devices operating at the same power supply voltage and within 5°C of each other within the operating temperature range.*

NOTE12 *Generator output characteristics for the f_{MAX}: Z_0 = 50Ω, $t_r = t_f$ < 1 ns, 50% duty cycle, 1.05 V to 1.35 V peak to peak. Output criteria: 60% / 40% duty cycle, VOL (max 0.4 V), VOH (min 2.7 V).*

NOTE13 *The capacitive load C_L, includes test fixture, probe and lumped capacitance.*

TEST CIRCUITS AND TIMING DIAGRAMS

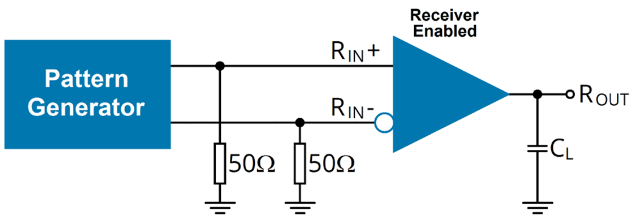


Figure 1. Receiver Propagation Delay and Transition Time Test Setup

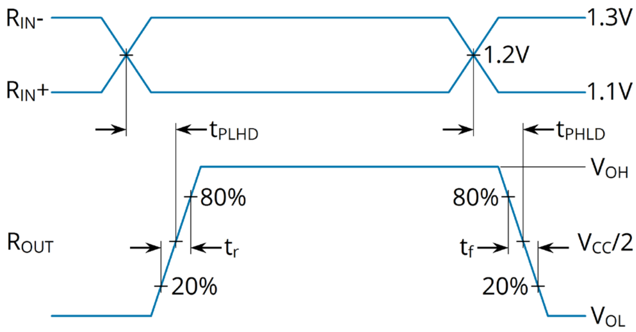


Figure 2. Receiver Propagation Delay and Transition Time Waveforms

TEST CIRCUITS AND TIMING DIAGRAMS (CONTINUED)

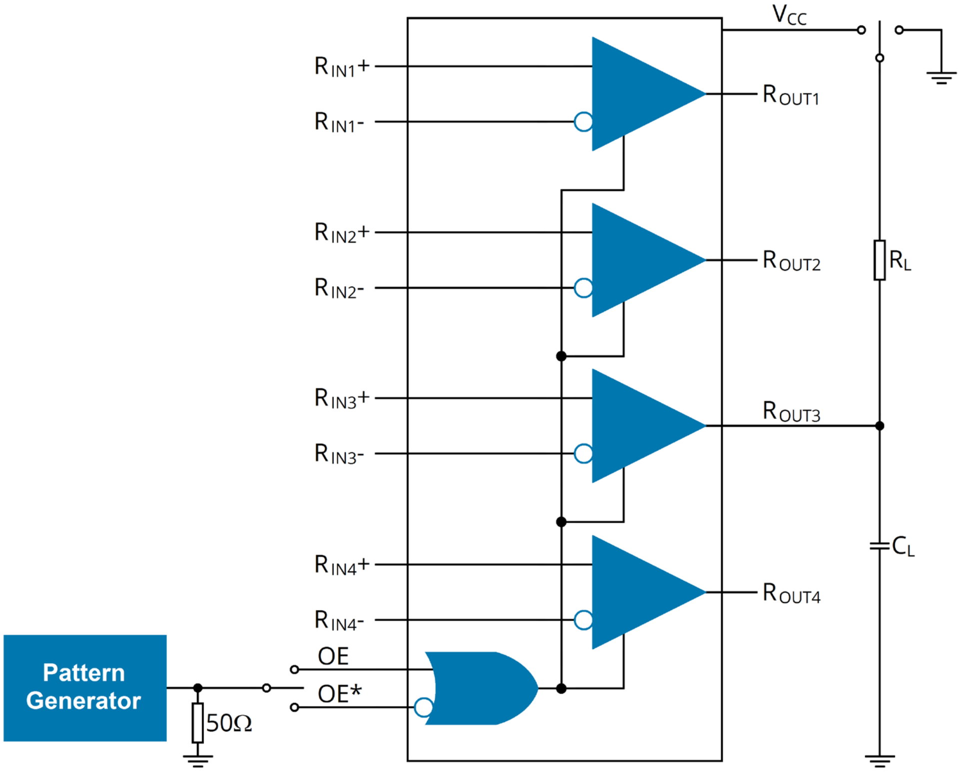


Figure 3. Receiver High-Z Delay Test Setup

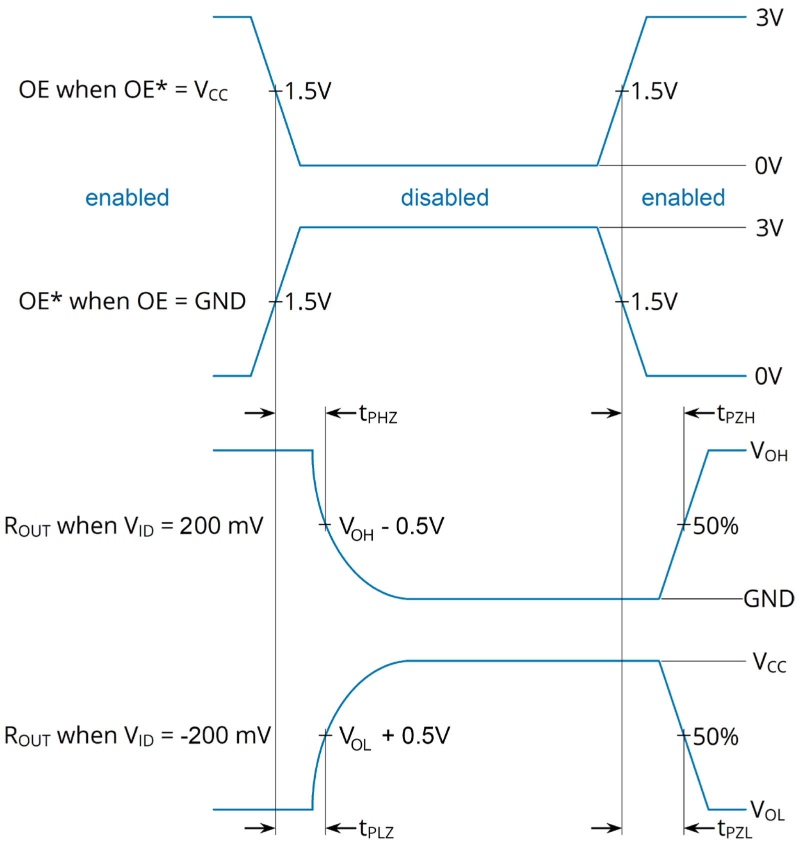


Figure 4. Receiver High-Z Delay Test Waveforms

APPLICATION INFORMATION

ABOUT LVDS

Due to bandwidth and power consumption, high speed communication links usually use differential signaling. In this area LVDS provides an outstanding performance to power ratio: It offers a high bandwidth at very low power consumption and low EMI. Therefore it is used extensively for audio and video transmission, ASIC and FPGA I/O, sensor data transmission, clock distribution and a lot more signaling tasks.

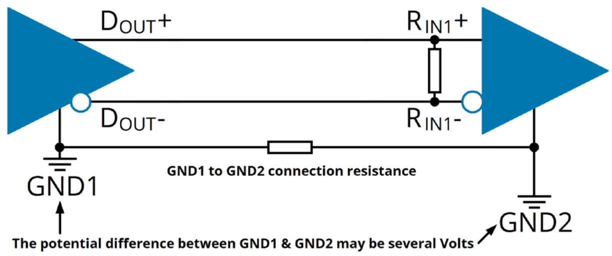


Figure 5. GND-potential difference

COMMON MODE

Having a look at a transmission line, usually there will be two grounds, one transmitter ground potential and one receiver ground potential. Defined by standard LVDS specification, the receiver input signal has to be between 0 and 2.4 Volts. Taking into account the typically at 1.2 Volts centered LVDS signal with a standard 400 millivolt differential signal this results in a maximum ground shift or noise margin of plus/minus 1 Volt. This means that steady-state differences as well as momentary shifts have to be lower than 1 Volt in absolute value. Usually this is enough margin, but under noisy conditions, at long distances or inadequate ground connection this may cause data transfer errors.

GROUND BOUNCE AND GROUND DRIFT

Large switching currents in an electrical system may result in a momentary voltage drop in supply voltage and/or in a local raise of the ground potential. In terms of the instantaneous ground potential shift this behaviour is known as ground bounce. This reaction to high currents may be reduced by proper design and size of ground and supply planes and the use of low resistive decoupling capacitors, but they cannot be eliminated totally. Another effect in this context is a steady-state potential difference between ground connections: Each connection generates a voltage drop which follows Ohm's Law (U = R * I). As a result the ground potential difference between a module and the main ground plane rises linearly with current and terminal resistance. Since the terminal resistance may increase by aging, the ground potential of the connected module may drift more and more resulting in a higher steady-state potential difference. In both situations, ground bounce and ground drift, the common mode difference between transmitter and receiver may exceed the specified +/- 1 Volt defined by the LVDS standard resulting in communication errors or even link interruption. These effects have already been reported in Avionics, Industrial applications, by telecommunication companies and automobile manufacturers.

POSSIBLE SOLUTION: AC COUPLING?

One possibility to eliminate common mode differences caused by ground potential issues is the use of coupling capacitors on both channels of the differential pair. But there is a big constraint: Capacitive coupling is only convenient for DC balanced data. This means that the data has to have an equal number of ones and zeros. But generally this is not the case for non-coded data, audio, video, sensor or control signals. And if the data would be coded in order to get a balanced signal, this would have an impact on the bandwidth. In case of 8b/10b coding the net data rate will decrease by 20%.

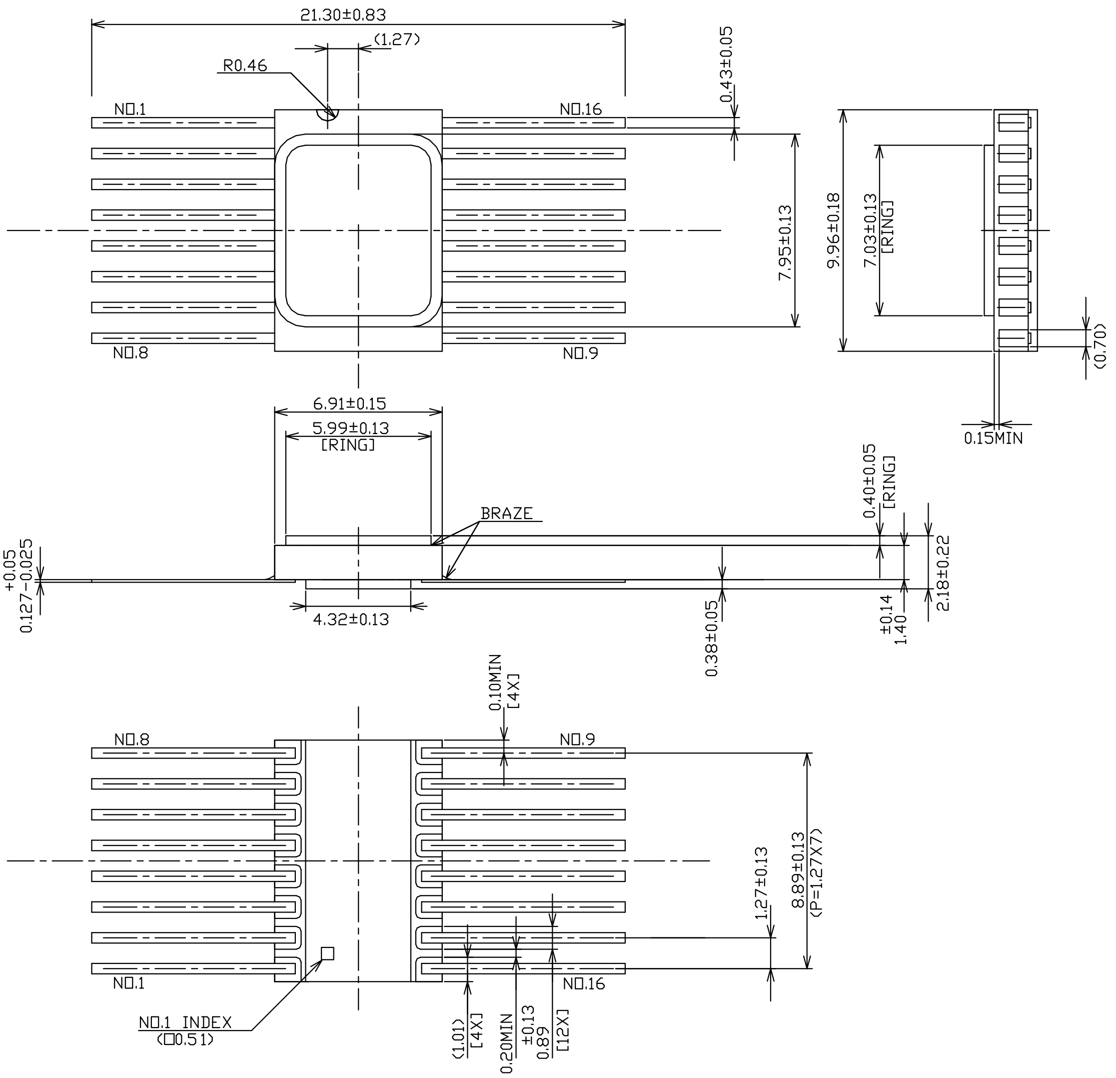
RS-485

In noisy environments and applications with known common mode issues usually the RS-485/422 is used due to its large swing differential standard which guarantees communication at common modes of -7 to +12 Volts. Its disadvantages are the low data rate and the poor bandwidth to power and EMI performance.

SPLVDS: COMBINING THE ADVANTAGES

Having a look at the LVDS standard, the noise margin may be sufficient on single PCBs or in small boxed systems. But in noisy environments or larger distributed systems or box-to-box communication, the small +/-1 V common mode window potentially leads to communication problems, particularly over the lifetime of the system. RS-485 offers a much better noise margin but shows very poor performance regarding power consumption, speed and EMI. The new Space IC SPLVDS series combines the benefits of LVDS and RS-485: It's fully compatible with the LVDS standard in terms of signal levels, speed, power and EMI, showing the same pinout and footprint as competitor devices. Additionally it provides an extended common mode of -7 to +12 Volt what finally makes it a perfect choice for harsh environments. Also it works as a high-performance replacement for RS-485 applications.

PACKAGE DIMENSION (16-LEAD FLATPACK)



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